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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,707	01/06/2004	Ming-Tung Lee	11809-US-PA	1706

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
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EXAMINER	
THOMAS, TONIAE M	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,707	LEE ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears n the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/707,707. Currently, claims 1-22 are pending.

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. *Claims 5, 4, 6, 14, 16, 19, 20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

The "insulating spacer" lacks antecedent basis (claim 14).

The scope of dependent claims 5, 6, 19, and 20 is unclear, since the "removing" steps in the claims are recited in "so that" clauses. For example, claim 5 recites the limitation, "wherein the antireflection layer includes inorganic material, so that the antireflection layer is not removed during removing the photoresist layer and the oxide layer is formed on sidewalls of the control gate. It is unclear if this claim requires the removing of the photoresist layer. Likewise, in claim 6, it is recited that the antireflection layer includes

organic material, so that the antireflection layer is simultaneously removed during removing the photoresist layer and the oxide layer is formed on top and sidewalls of the control gate. It is unclear if claim 6 actually requires the removing of both the photoresist layer and the antireflection layer and forming the forming of the oxide layer on the top and sidewalls of the control gate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. *Claims 1-3, 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (US 2003/0032224 A1) in view of Willer (US 6,674,132 B2).*

The Sung et al. patent (Sung) discloses a method for fabricating a non-volatile memory (figs. 2, 3, and accompanying text). The method comprises the following steps: providing a substrate 200 with a stacked structure having a control gate 214, a barrier layer 206, a trapping layer 204, and a tunneling layer 202 (fig. 2 or 3); forming an insulating spacer 216 on a sidewall of the stacked structure (fig. 2 or 3); and forming an ultraviolet-resistant lining layer 220/270 over the surface of the stacked structure (fig. 2 or 3, par. 18, lines 9-13, and par. 20, lines 1-7).

In one embodiment, the insulating spacer 216 is a silicon oxide spacer (par. 17, lines 9-15). In one embodiment, the ultraviolet-resistant lining layer is a silicon nitride lining layer (par. 18, lines 9-13). A source/drain region 228, 224 is formed in the substrate at each side of the stacked (fig. 2 or 3).

Sung lacks anticipation in not teaching that an antireflection layer covers the stacked structure on top, and that an oxide layer is formed on an exposed surface of the of the control gate. Willer discloses a method for fabricating a non-volatile memory (figs. 1-4 and accompanying text). The method comprises forming an antireflection layer 7 on a stacked structure having a control gate 5, 6, a barrier layer 4, a trapping layer 3, and a tunneling layer 2 (fig. 3, col. 6, lines 44-61, and col. 7, lines 12-26), and forming an oxide layer on an exposed surface of the control gate (fig. 3 and col. 7, lines 27-35). The antireflection layer includes inorganic material (col. 6, lines 59-61).

One having ordinary skill in the art, at the time the invention was made, would have been motivated to modify Sung in view of Willer by forming an antireflection layer 7 on a stacked structure and forming an oxide layer on an exposed surface of the control gate, as taught by Willer, because: forming an antireflection layer on the stacked structure prior to patterning the stacked structure reduces the standing wave effect, which occurs when actinic light waves propagate through a resist film down to the substrate, and are reflected back up through the resist;[i] and forming an oxide layer on the exposed surface

of the control gate 214 in Sung protects the gate during a subsequent etching step to form the sidewall spacers 216.

5. *Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung in view of Willer as applied to claim 3 above, and further in view of Bhattacharyya (US 6,743,681 B2).*

Sung does not teach that the silicon nitride lining is formed using a PECVD process. However, Bhattacharyya teaches using a PECVD process to form silicon-rich nitride layer, wherein the PECVD process uses a reacting gas including a SiH_4 gas, an NH_3 gas, and a N_2 gas (col. 8, lines 29-52).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the silicon nitride lining using a PECVD process, as taught by Bhattacharyya, since the silicon nitride formed is a silicon-rich nitride layer.

Bhattacharyya does not teach the power and gas flow rates used during the PECVD process. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a process power between 370W and 410W and a SiH_4 gas with a flow rate between 50 sccm and 60 sccm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

6. *Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. in view of Willer as applied to claim 1 above, and further in view of Gupta et al. (US 5,910,453).*

Willer does not teach that the antireflection layer includes an organic material. Gupta discloses using an organic antireflection layer 14 in a patterning process (figs. 1-4 and accompanying text). The antireflection layer is formed on an underlying layer 18 to be patterned (fig. 1 and col. 5, lines 57-65).

Since both inorganic and organic materials are used as antireflection layers, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to substitute the inorganic antireflection layer of Willer with the organic antireflection layer of Gupta.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung in view of Willer as applied to claim 1 above, and further in view of Wolf. Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).

The oxide layer 8 in Willer is formed by an oxidation process (col. 7, lines 27-34). However, Willer does not teach that the oxidation process is a thermal oxidation process. Wolf teaches the formation of an oxide using a thermal oxidation process (page 198 – par. 1, lines 1-8).

One having ordinary skill in the art would have been motivated to modify the combination of Sung and Willer, at the time the invention was made, by forming the oxide layer using a thermal oxidation process because thermal

oxidation produces oxide films with controlled thickness and Si/SiO2 interface properties (Wolf – page 198, par. 1, lines 5-7).

8. *Claims 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. in view of Noguchi et al. (US 2004/0094793 A1).*

Sung discloses a fabrication process for metal interconnects (figs. 3 and accompanying text). The method comprises the following steps recited in claim 9: providing a substrate 200, the substrate having a conducting structure 214; forming a dielectric layer 272, 274, 275, 278 on the substrate to cover the conducting structure; forming a contact window 284 in the dielectric layer, the contact window being electrically connected to the conducting structure; and forming a conducting line structure 282 on the dielectric layer, the conducting line structure being electrically connected to the contact window.

Sung lacks anticipation in not teaching the steps of forming a low surface charge lining layer on surfaces of the dielectric layer and the conducting line structure, wherein the low surface charge lining layer is one of a silicon oxide lining layer and a silicon nitride lining layer; and forming a second dielectric layer on the low surface charge lining layer. Noguchi discloses a fabrication process, wherein the fabrication process comprises forming a silicon oxide layer 16 over a dielectric layer 14, and forming a second dielectric layer 17 on the silicon oxide layer (fig. 1 and par. 47). The silicon oxide layer 16 is an interlayer dielectric layer, and the second dielectric layer is a passivation layer.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Sung in view of Noguchi by forming a silicon oxide layer on the surfaces of the dielectric layer and conducting line structure, and forming a passivation layer on the silicon oxide layer, as taught by Noguchi, because: forming a silicon oxide layer over the dielectric layer and conducting line structure electrically isolates the conducting line structure from subsequently formed metallization layers, and forming a passivation layer on the silicon oxide layer protects the conducting structure from mechanical and chemical damage during back-end processing.[ii]

9. *Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. in view of Noguchi et al. as applied to claim 9 above, and further in view of Wolf et al. Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).*

Noguchi does not teach that the silicon oxide lining is formed using a PECVD process. However, Wolf teaches using a PECVD process to form a silicon oxide layer, wherein the PECVD process uses a reacting gas including a SiH_4 gas and nitrous oxide (N_2O) (page 184 – par. 4, line 1 – par. 6, line 5). A silicon oxide layer formed using PECVD is very conformal, and has good adhesion (page 184 – par. 6, lines 3-5).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the silicon oxide lining using a PECVD

process, as taught by Wolf, since the silicon oxide formed using PECVD has good step coverage and good adhesion to metals.

Wolf does not teach the power and gas flow rates used during the PECVD process. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use a process power between 80W and 120W and a SiH_4 gas flow rate between 20 sccm and 30 sccm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

10. *Claims 13-15, 17, 19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. in view of Willer and Noguchi et al.*

As discussed above, Sung discloses a method for fabricating a non-volatile memory. Sung lacks anticipation in not forming an antireflection layer on the stacked structure; forming an oxide layer on an exposed surface of the of the control gate; forming a low surface charge lining layer on surfaces of the dielectric layer and the conducting line structure, wherein the low surface charge lining layer is one of a silicon oxide lining layer and a silicon nitride lining layer; and forming a second dielectric layer on the low surface charge lining layer.

Willer discloses a method for fabricating a non-volatile memory (figs. 1-4 and accompanying text). The method comprises forming an antireflection layer 7 on a stacked structure having a control gate 5, 6, a barrier layer 4, a trapping

layer 3, and a tunneling layer 2 (fig. 3, col. 6, lines 44-61, and col. 7, lines 12-26), and forming an oxide layer on an exposed surface of the control gate (fig. 3 and col. 7, lines 27-35). The antireflection layer includes inorganic material (col. 6, lines 59-61).

Noguchi discloses a fabrication process, wherein the fabrication process comprises forming a silicon oxide layer 16 over a dielectric layer 14, and forming a second dielectric layer 17 on the silicon oxide layer (fig. 1 and par. 47). The silicon oxide layer 16 is an interlayer dielectric layer, and the second dielectric layer is a passivation layer.

One having ordinary skill in the art, at the time the invention was made, would have been motivated to modify Sung in view of Willer by forming an antireflection layer 7 on a stacked structure and forming an oxide layer on an exposed surface of the control gate, as taught by Willer, because: forming an antireflection layer on the stacked structure prior to patterning the stacked structure reduces the standing wave effect, which occurs when actinic light waves propagate through a resist film down to the substrate, and are reflected back up through the resist; and forming an oxide layer on the exposed surface of the control gate 214 in Sung protects the gate during a subsequent etching step to form the sidewall spacers 216. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Sung in view of Noguchi by forming a silicon oxide layer on the surfaces of the dielectric layer and conducting line structure, and forming a passivation layer on the

silicon oxide layer, as taught by Noguchi, because: forming a silicon oxide layer over the dielectric layer and conducting line structure electrically isolates the conducting line structure from subsequently formed metallization layers, and forming a passivation layer on the silicon oxide layer protects the conducting structure from mechanical and chemical damage during back-end processing.

11. *Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. in view of Willer and Noguchi et al. as applied to claims 15 and 17 above, respectively, and further in view of Bhattacharyya.*

Sung does not teach that the silicon nitride lining is formed using a PECVD process. However, Bhattacharyya teaches using a PECVD process to form silicon-rich nitride layer, wherein the PECVD process uses a reacting gas including a SiH_4 gas, an NH_3 gas, and a N_2 gas (col. 8, lines 29-52).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the silicon nitride lining using a PECVD process, as taught by Bhattacharyya, since the silicon nitride formed is a silicon-rich nitride layer.

Bhattacharyya does not teach the power and gas flow rates used during the PECVD process. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a process power between 370W and 410W and a SiH_4 gas with a flow rate between 50 sccm and 60 sccm, since it has been held that where the general conditions of a claim are

disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

Noguchi does not teach that the silicon oxide lining is formed using a PECVD process. However, Wolf teaches using a PECVD process to form a silicon oxide layer, wherein the PECVD process uses a reacting gas including a SiH_4 gas and nitrous oxide (N_2O) (page 184 – par. 4, line 1 – par. 6, line 5). A silicon oxide layer formed using PECVD is very conformal, and has good adhesion (page 184 – par. 6, lines 3-5).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the silicon oxide lining using a PECVD process, as taught by Wolf, since the silicon oxide formed using PECVD has good step coverage and good adhesion to metals.

Wolf does not teach the power and gas flow rates used during the PECVD process. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use a process power between 80W and 120W and a SiH_4 gas flow rate between 20 sccm and 30 sccm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

12. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. in view of Willer and Noguchi et al. as applied to claim 13 above, and further in view of Gupta et al.

Willer does not teach that the antireflection layer includes an organic material. Gupta discloses using an organic antireflection layer 14 in a patterning process (figs. 1-4 and accompanying text). The antireflection layer is formed on an underlying layer 18 to be patterned (fig. 1 and col. 5, lines 57-65).

Since both inorganic and organic materials are used as antireflection layers, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Sung, Willer, and Noguchi, by substituting the inorganic antireflection layer of Willer with the organic antireflection layer of Gupta.

13. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung in view of Willer and Noguchi as applied to claim 13 above, and further in view of Wolf. Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).

The oxide layer 8 in Willer is formed by an oxidation process (col. 7, lines 27-34). However, Willer does not teach that the oxidation process is a thermal oxidation process. Wolf teaches the formation of an oxide using a thermal oxidation process (page 198 – par. 1, lines 1-8).

One having ordinary skill in the art would have been motivated to modify the combination of Sung, Willer, and Noguchi, at the time the invention was made, by forming the oxide layer using a thermal oxidation process because

thermal oxidation produces oxide films with controlled thickness and Si/SiO2 interface properties (Wolf – page 198, par. 1, lines 5-7).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ
27 June 2004

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[i] Wolf et al., « Litography I : Optical Resist Materials and Process Technology, » Silicon Processing for the VLSI Era – Vol. 1: Process Technology, (page 438, par. 4, lines 1-2).
[ii] Wolf, « Multilevel-Interconnect Technology for VLSI and USLI, » Silicon Processing for the VLSI Era – Vol. 2: Process Integration, (page 273 - §4.8, lines 1-3).

Mary Wilczewski
Primary Examiner